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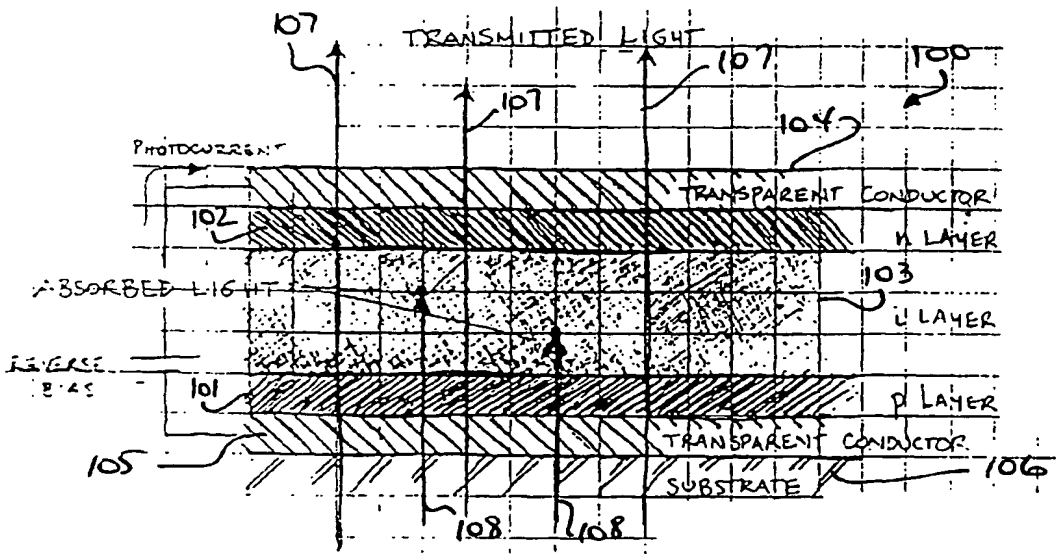

(57) Abstract: Materials suitable for fabricating optical monitors include amorphous, polycrystalline and microcrystalline materials. Semitransparent photodetector materials may be based on silicon or silicon and germanium alloys. Conductors for connecting to and contacting the photodetector may be made from various transparent oxides, including zinc oxide, tin oxide and indium tin oxide. Optical monitor structures based on PIN diodes take advantage of the materials disclosed. Various contact, lineout, substrate and interconnect structures optimize the monitors for integration with various light sources, including vertical cavity surface emitting laser (VCSEL) arrays. Complete integrated structures include a light source, optical monitor and either a package or waveguide into which light is directed.

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A SEMITRANSPARENT OPTICAL DETECTOR INCLUDING A SILICON AND GERMANIUM ALLOY AND METHOD OF MAKING

Background

1. Field of the Invention

The present invention relates generally to devices for monitoring the performance of optical systems. The present invention relates more particularly to devices for monitoring the performance of laser light sources used in communications and computation systems.

2. Related Art

The vertical cavity surface-emitting laser (VCSEL) is a relatively recent innovation in laser technology. It is part of a general class of devices called "surface emitting light emitting devices" (SLEDs) that have significant manufacturing and packaging advantages over conventional edge-emitting devices.

Semiconductor diode lasers have been produced for over a decade and are used extensively in both communications and in optical storage devices such as compact disks (CDs) and digital versatile disks (DVDs). The vast majority of these devices, however, rely on edge-emitting, e.g., Fabry-Perot or distributed feedback (DFB), lasers. These lasers are constructed on semiconductor wafers in such a way that when the wafer is diced, light is emitted from the cut edges. Edge emitting devices have a number of drawbacks: first, each laser takes a relatively large area on the semiconductor wafer, increasing cost; second, lasers cannot be tested until after they have been diced into individual units; third, linear arrays of lasers are more difficult to produce in high densities and two-dimensional arrays are altogether impossible to fabricate. The construction and fabrication of these lasers, however, is well known, and prices have benefited from large production volumes needed to satisfy the CD and DVD markets.

VCSEL laser cavities – rather than being patterned in the wafer plane, in a few layers of semiconductor – are patterned orthogonally to the wafer as many layers of semiconductor are deposited. The resulting lasers emit light perpendicularly to the surface of the wafer, and may be patterned in extremely high densities, either as individual devices or as one or two dimensional arrays. The result is a laser device that is inherently less expensive to produce than edge-emitting lasers. In addition, the

Various solutions have been developed for controlling optical output of diode lasers. The first category of solutions has to do with temperature monitoring and control. The idea is that one can either monitor temperature – or control it directly – of the laser device, and therefore eliminate drift in threshold current and slope efficiency tied to temperature fluctuations. The simplest solution is to place a temperature-monitoring device near the laser and to use the signal from this device to adjust the laser bias current and possibly the laser modulating current according to a pre-set formula determined from statistical sampling of the laser devices.

Another solution, which is used extensively in high-end communications modules employing edge-emitting lasers, is active control of laser temperature. The laser is placed on a substrate that has incorporated both a temperature-measuring device and a cooling device – most often a semiconductor heat pump such as a Peltier junction – that, through a control loop, keep the laser base at a constant temperature where the threshold current and slope efficiency are known (and usually optimal).

Thermal control solutions require significant space and power, and although they may be suitable for long-haul communications applications, such solutions are generally unacceptable in local-area or interconnect components where space is at an extreme premium.

Thermally-based solutions do not by themselves solve the problem of laser performance degradation over its operating lifetime. They can only compensate for changes in the ambient temperature, which, although important, are far from the only factor affecting laser optical output for a given current.

The most accurate way of controlling power output from the laser is to monitor the optical output directly. A class of technologies has been developed to monitor this output for both edge- and vertically-emitting semiconductor lasers.

Direct optical power monitoring for edge-emitting lasers is relatively straightforward due to the fact that these diode lasers emit light from both front and back facets. This allows the laser to be placed in an assembly where one aperture, at the front facet, provides the useful light for the application, while the other aperture provides light to a photodiode that is aligned precisely with the back facet. The usual technology used for this alignment is referred to as a silicon workbench. A silicon wafer has a surface patterned with mechanical alignment grooves using micromachining processes to

additional VCSEL is constructed, at the end of array for the sole purpose of monitoring power output. However, this technique has severe drawbacks. Not only will it result in different average power levels coming from the lasers and, indeed, a higher required overall bias current than necessary in order to insure reliable function over lifetime, but may result in such disparities in power that an eye safety hazard results. This is of particular concern with a WDM system where multiple signals will travel through a single fiber to their destination, and aggregate optical power is measured to determine safety standards.

Another major drawback of current backreflection power monitors is the fact that light emanating from the VCSEL is not uniformly measured by the detector. Each VCSEL emits light not in a single beam or direction, but in various intensities in different directions off-axis, typically in a circular pattern. Typically VCSELs have beam divergence of 5-20°, with optical power unevenly distributed both by angle and radius in the beam. This poses a problem for an optical monitor that reflects part of the emitted light into a photodiode. This means that only a few of the modes of a VCSEL are measured by the photodiode. From VCSEL to VCSEL, then, the photocurrent produced in the detector will be vastly different, even for identical VCSEL output powers. The impractical result is that each VCSEL/monitor unit must be individually calibrated after assembly in order to know the relation between photodiode current and actual optical power produced by the VCSEL. This uncertainty is reflected in current product data sheets by the "photocurrent at typical VCSEL power," which varies from min to max by as much as a factor of 10. Moreover, the relative intensities of the modes emitted by a VCSEL will change over temperature and age which means that the conditions observed during calibration may not exist over the entire operating lifetime of the VCSEL, and significant distortions of the power feedback signal may result over time. Other issues such as the mechanical and optical stability of the semireflective window used to direct light back to the photodetector will affect measurement as well. For example, dust on the outside of the window may cause significantly higher backreflection, leading to an overestimate of delivered laser power.

Current VCSEL/monitor units must exceed a certain minimum size because the partially-reflective window used to direct some light back towards the photodetector must be a set distance away in order to take advantage of the VCSEL's natural beam

required in order to minimize dark current while preserving functionality in the application-specific device. A particular problem is the leakage on the edges of the device.

In many cases it is desirable to build tall microelectronic structures for sensor or actuator applications. For many of these applications a top conductive contact with a lineout to a contact pad is required. When the conductor used for this connection is relatively thin when compared to the structure's height and is deposited by a directional method that preferentially deposits on surfaces parallel to the substrate broken connections often result.

Using standard metal deposition techniques like electron-beam deposition or thermal evaporation, metal is deposited perpendicular to the substrate, and therefore preferentially coats surfaces parallel to the plane of the substrate. An immediate potential solution was to use very thick layers of metal to form the contact once the layer is thick enough it will reach over the edge of the PIN stack; this fix, however, brings with it other problems when working with thin films. In particular, the film stress induced by such a thick layer will tend to peel off the entire photodetector structure.

In many cases it is desirable to build "tall" microelectronic structures for sensor or actuator applications. For many of these applications a top conductive contact with a lineout to a contact pad is required. When the conductor used for this connection is relatively thin when compared to the structure's height, and is deposited by a directional method that preferentially deposits on surfaces parallel to the substrate, broken connections often result.

Another problem is because the entire PIN structure was extended for large areas under the insulating layer and contacts i.e., areas that do not contribute to the intended photoresponse of the device, the dark current exhibited by the devices rose significantly for two reasons: (1) there is a much larger bulk of PIN stack that will produce purely thermal currents, particularly at higher temperatures and (2) the leakage currents produced along the extended edges of the structure rise. These effects are particularly noticeable when a high reverse bias is used to increase the response of the detector to light.

Brief Description of the Drawings

In the drawings in which like reference designations indicate like elements:

Fig. 1 is a cross-section of a PIN diode according to some aspects of the invention;

Fig. 2 is a graph of quantum efficiency versus wavelength for amorphous silicon and amorphous silicon-germanium alloys;

Fig. 3 is a cross-section and graph showing the effect of germanium concentration in the intrinsic layer of a PIN diode;

Fig. 4 is a schematic cross-section of a system including a light source and a semitransparent PIN diode;

Fig. 5 is a schematic cross-section of a system including a light source and a flip bonded PIN diode on a substrate;

Fig. 6 is a schematic cross-section of a light source and a semitransparent PIN diode constructed on the surface of the light source;

Fig. 7 is a light source in a package including a semitransparent PIN diode;

Fig. 8 is a schematic cross-section of a PIN diode including an edge passivation layer;

Fig. 9 is an edge passivated PIN diode structure showing a first metallization system;

Fig. 10 is a schematic cross-section of an edge passivated PIN diode showing a second metallization system;

Fig. 11 is a schematic cross-section of an edge passivated PIN diode showing a third metallization system;

Fig. 12 is a plan view of a contact structure for an edge passivated PIN diode;

Fig. 13 is a schematic cross-section of an edge passivated PIN diode having the contact structure illustrated in Fig. 12;

Figs. 14 and 15 are plan views of PIN diode arrays employing the contact structure of Figs. 12 and 13;

Fig. 16 is a schematic cross-section of an edge passivated PIN diode including a different ring contact structure;

Fig. 17 is a plan view of the PIN diode and contact structure of Fig. 16;

various materials and structures are described in relation to a number of preferred combinations. However, it will then be apparent that other combinations of the same materials and structures are suggested by the described combinations. All such combinations are contemplated as within the scope of this disclosure.

Basic Materials

In order to build semitransparent optical detectors, semitransparent materials are required. In order to use conventional crystalline silicon semiconductors one would need to cut a single-crystal wafer so thin that most of the monitored beam could pass through the wafer and a detector patterned on it using conventional integrated-circuit processes. The advantage of this method is that conventional semiconductor processing techniques could be used to fabricate the photodiode on the wafer. However, the process is relatively expensive. Only very limited tuning is possible when photodetectors are formed using conventional processing, and crystalline silicon in general has very poor absorption, so that relatively thick layers may be required to produce sufficient photocurrent for a control signal.

The advantages of using thin-film, directly-deposited semiconductors for such detectors are multiple and powerful: first, a variety of substrates, including low-cost glass and perhaps even the VCSEL wafer, may be used; second, these semiconductors may be processed in very large areas; third, because the semiconductor is deposited directly, the layers of the material may be very precisely tuned for the application – which will help to meet all the requirements of the much-needed semitransparent laser monitor. In addition, the ability to fabricate not only amorphous but also microcrystalline and polycrystalline semiconductors in thin-film form gives the designer a high degree of flexibility in tuning the photodetector for specific wavelengths, signal-to-noise requirements, thicknesses, transmission, etc.

Several potential devices could serve as photodetectors: PN junctions, PIN diodes, phototransistors, photodarlingtons, and metal-semiconductor, i.e., Schottky diode junctions. All of these devices are theoretically possible to construct in a thin-film semiconductor version. For simple devices, PN junctions and PIN diodes are viable alternatives. PN junctions, however, do not trap sufficient light to produce feedback currents that, without amplification, could be used by current laser driver chips.

signal at 850nm. A comparison of the quantum efficiency of the amorphous-silicon germanium device 201 with that of an amorphous-silicon only device 202 is shown in Fig. 2. In addition, the germanium concentration was optimized in such a way as to keep the dark current to low levels, producing over 100:1 SNR ratios at a range of reverse bias voltages up to approximately 2-3V, roughly. This result for a semitransparent detector represents a major advance in the state of the art in VCSEL monitor technology because it allows for capture of all laser modes, extremely compact integration with packaging or the laser itself, and continued use of chipsets developed for use with backreflection monitors.

Semitransparent PIN devices constructed from amorphous silicon - germanium alloys exhibit high levels of absorption in the 850nm range for optical communications lasers and a relatively low saturation point under reverse bias. These devices can be constructed using a graded concentration of germanium, where there is no Ge present in the alloy at the P and N interfaces, and the concentration rises in the center of the I layer. The result is a smooth valence band transition to the N and P layers, while photon absorption at the wavelength of interest is high in the center of the layer. A depiction of the graded concentration 301 together with the smoothly-varying (and narrowing) bandgap 302 is shown in Fig. 3. The grading 301 eliminates the bandgap mistmatch 303 which causes a pileup of charge carriers at the interfaces when the electric field is low, which in turn leads to unwanted carrier recombination at the interface and lower photocurrent. As a result of the grading 301, the PIN photodiode 100 may be run at reverse bias voltages as low as 1V, or even unbiased and still produce a over 75% of the photocurrent observed at 2-3V reverse bias. This result is highly beneficial as optoelectronic circuits migrate to lower-voltage operation.

Making the Basic Materials

The exemplary semitransparent PIN device 100 can be fabricated using equipment such as that used to build amorphous silicon solar cells in large quantities. For example, devices can be fabricated using a plasma-enhanced chemical vapor deposition (PE-CVD) process, although other well-known methods exist for depositing amorphous silicon. The amorphous silicon device itself is fabricated as follows, with the specific process parameters dependent on the precise machine used:

1. In a vacuum, deposit a transparent conductor on a substrate that is transparent to the wavelength of interest.

2. Without removing the substrate from vacuum, and having the substrate at an elevated temperature throughout the process, perform the following steps to fabricate the semiconductor detector layers:

a. deposit a relatively thin p-doped layer of amorphous silicon using commonly-known dopant such as boron;

b. deposit a relatively thick intrinsic layer of amorphous silicon with germanium provided by germane (GeH_4), at up to 100% germane as a total of entire gas volume, depending on machine and process specifics (the germane concentration should be varied from about 0% concentration at the P-I and N-I interfaces, with a ramp up at both interfaces to the desired maximum level depending on exact wavelength of interest which is then maintained for a substantial portion of the I layer; and

c. deposit a relatively thin N-doped layer of amorphous silicon using a dopant such as phosphorous.

3. Deposit a transparent conductor on top of the resulting PIN stack, to serve as the top contact for the device.

Basic Structures

In order to produce devices economically which possess various desired characteristic, we have invented several new basic structures. These structures address issues relating to reducing the dark current, making electrical contact with the device, and other.

In order to control and reduce dark current, as shown in Fig. 8, an integrated, insulating shell 801 can be constructed around our photodetectors according to aspects of the invention that minimizes edge currents around the photodetector device. After depositing a pattern bottom contact layer 105, if needed, the photodetector stack 101, 102, 103, and the top transparent conducting window 104, if needed an insulating layer 801 can be added to the device. This insulating layer 801 can optionally then be removed from the window area 802 and from the point 803 where contact must be made to the bottom contact. In this construction, the layer 801 acts not only as the passivating edge layer for the photodetector device, but also as an insulating layer 801 between top and bottom contacts and lineouts (not shown). Among the materials that can be used for

unobstructed. This restricts the type of conductive material that may be used at either end of the photodetector. Generally a transparent conductive oxide will be used to make contact 104, 105 to the top 102 and bottom 101 layers of the detector 100. These oxides, however, have limited conductivity, particularly when they are made relatively thin. If the aperture is small and the top 102 and or bottom 101 layers of the detector are made of non-amorphous (microcrystalline or polycrystalline) material, which has better conduction, the transparent conductors 104, 105 may be left off altogether. However, it is desired to minimize the product of distance and resistivitiy from good conductive leads to the locations in the device where electron-hole pairs are created.

The structure next described, which provides such a contact, requires only a single deposition and patterning step for the metal layer, which is applied as one of the final layers in the semitransparent PIN structure. The structure of these contacts minimizes the average distance from the point of carrier generation to a metal lead while ensuring proper isolation for reliable measurements. In addition, the contact structure minimizes any capacitive effects that might occur.

The structure consists of an inner top contact ring 1201 and an outer bottom contact ring 1202, as shown in Figs. 12 and 13. The inner ring 12 contacts the top of the PIN stack, or the transparent conductor 104 that has been applied to the top of the stack. The outer ring 1202 contacts, through an arc-shaped via 1301 patterned in an insulating layer, the bottom conducting layer 105, which may be either a transparent conductor 105 covering the entire PIN aperture or any conductor that contacts the bottom layer 101 of the PIN. The metal contacts 1201, 1202 may be fabricated using aluminum, chromium, or other conductors compatible with standard deposition processes such as thermal or e-beam evaporation or sputtering. After a thin-film conductor has been formed, it may be most effective to plate it with a good contact layer (electroless gold plating, for instance) to guarantee contact reliability in the final assembly. The ring-shaped conductors 1201, 1202 minimize the distance from points on the detector to contacts for outside control circuitry (or to integrated circuitry). A ring also ensures the highest uniformity in response to different optical paths through the detector. Representative arrays using the described structures are shown in Figs. 14 and 15.

photoresist is etched away. The etch process continues, stopping at the bottom conductor and the top conductor, though timing must be accurate to ensure the sloped PIN stack is not eliminated completely. An insulating layer (Fig. 22, 2202) and a conductor layer (Fig. 22, 2203) are patterned on to the tapered PIN structure. The conductor (Fig. 22, 2203), deposited by standard e-beam or evaporation techniques, remains integral between the contact pad and the top PIN contact.

In order to improve the performance by restricting the photoelectrically active region and the electrically active region of the device, embodiments of the invention including structures where the active area is defined by the top and/or bottom contacts to the PIN stack are now described. These contacts may be defined in two ways. They may be defined through patterning of the conductor itself or through patterning of an insulating layer.

An example of the former is shown in Fig. 23. In this case, the top transparent conductive layer 2301 has been patterned to electrically contact a limited area 2302 in a large-area PIN stack 2303. The advantage of this structure is that it can be constructed using relatively simple processing. The disadvantage is that the top transparent conductive layer 2301 may be so thick as to form an edge that may not be bridged properly by the metal line-out. This can be overcome by careful conventional processing or by other structures described herein.

Examples of the latter include defining a masking layer of an insulating material either at the bottom or top surface of the PIN stack. An immediate advantage of this structure for confining the photodetector is that it maximizes the ratio of the optically active area to the electrically active one, which results in higher contrast between the photocurrent and the dark current in reverse-biased conditions.

The top mask structure is illustrated in Fig. 24. In this version the entire stack 2401 is deposited on a substrate 2402 coated with a conductor 2403, which may be a transparent conductor 2403. Passivation layer 2404 is applied and a window 2405 is etched to define the active area 2406. The transparent conductive layer 2407 is applied over the window, overlapping the transparent conductive layer 2404. Although there may still be some a step for the metal line-out 2408 at the edge of the transparent conductive layer 2407, this is not problematic because it is a conductor-conductor

After fabricating the passivating layer, the device needs metallization. Two metal traces are patterned in such a way that they contact the transparent conductor or, in the case where no transparent conductor is required, the top of the PIN stack through the aperture in the passivating layer on top of the PIN stack; and the bottom conductor through the via patterned in the passivating layer. The metal contacts correspond to the circuit wires drawn schematically in Fig. 1. The device is now protected significantly against edge currents and is ready to function as an optical power monitor for VCSELs and other devices.

Next, three methods of fabricating a semitransparent PIN photodiode with transparent conductors are described. The are described in the order of least to most complex, together with the advantages of each.

First, a method of making the structure of Fig. 9 is described.

1. Blanket-coat substrate 106 with bottom transparent conductor 105.
2. Deposit semitransparent PIN stack 101, 102, 103.
3. Deposit top transparent conductor 104.
4. Photolithographically pattern and etch top transparent conductor 104.
5. Use patterned top transparent conductor 104 as mask to etch PIN stack 101, 102, 103.
6. Deposit and pattern passivating/insulating layer 801.
7. Deposit and pattern metal contacts 901, 902 to top and bottom transparent conductors 104, 105.

Next, a method is described in which application of the top transparent conductor is done after passivation resulting in a slightly larger aperture, and the sides of the PIN stack potentially are electrically cleaner because a top transparent conductor is not present during patterning, resulting in lower edge dark currents. The steps for this process, which produces the structure of Fig. 10, are as follows:

1. Blanket-coat substrate 106 with bottom transparent conductor 105.
2. Deposit and photolithographically pattern the semitransparent PIN stack 101, 102, 103.
3. Deposit and pattern passivating/insulating layer 801.
4. Deposit top transparent conductor 1002.
5. Photolithographically pattern and etch top transparent conductor 1002.

semiconductor of reasonable conductivity, for example, microcrystalline or polycrystalline thin film, is used for the bottom layer of the PIN, as in Figs. 16 and 17.

1. The conductor is deposited in one step following deposition and patterning of the bottom transparent conductor, the PIN stack, the top transparent conductor, and the insulating/passivating layer, as described above. The conductor is patterned to form an inside ring matching the aperture of the PIN detector, contacting the top transparent conductor on the edge where it is covered by the insulating/passivating layer, or, in an alternative construction, where it covers the insulating layer. The outer conductor is patterned in a crescent shape that leaves just enough space for a lineout from the inner ring. This outside crescent sits on top of a trench that has been patterned in the insulator, giving a contact to the bottom transparent conductor around the majority of the detector. In the resulting structure, as shown in Fig. 13, the bottom transparent conductor should be optimized for higher conductivity to compensate for a larger mean distance to carry current between the detector and metal conductor, and the top conductor should be optimized for optical properties. Note that this corresponds to previously established needs, as the optical properties of the top transparent conductor as an anti-reflective coating are already considered.

2. Devices lacking transparent conductor layers will depend partly on a very small aperture to ensure sufficient conduction of generated electrons to control circuitry. The ideal design for such a device relies on two layers of conductive metal to sandwich the PIN device. In this design, it is optimal to make the top and bottom conductor apertures roughly the same diameter, or slightly skewed to account for the anticipated spread of a beam passing through the device. The processing is as previously described. The bottom metal layer is deposited and patterned into a ring with a lineout first, then the PIN stack and the insulating/passivating layer, possibly with a top transparent conductor either between the PIN and the insulator or on top of the insulator, then the second, i.e., top, layer of metal deposited and patterned into a top ring with lineout. Note that holes in the insulator are opened up during patterning to expose any pads needed to contact the bottom of the PIN. One advantage of this two-layer metal structure is that the bottom layers of an entire array of devices may be interconnected easily under the insulating layer. The resulting structure is shown in Figs. 16 and 17.

With higher bandwidth in the laser power monitor, intelligent circuitry may be integrated to monitor and adjust the relative intensities of high intensity and low intensity emissions representing logic levels "zero" and "one", or an entire grayscale for display, imaging, and other applications. Amorphous and microcrystalline materials are limited by electron and hole mobility to provide relatively long response times. Such devices are fine for monitoring average optical power over relatively long, e.g., microsecond-scale, periods. For faster response times, however, different materials must be employed.

A faster device embodying the invention is a semitransparent PIN photodiode fabricated using polycrystalline silicon. Polycrystalline silicon PINs have higher bandwidths than their amorphous and microcrystalline counterparts, and in addition are able to generate adequate signals at higher wavelengths. The device now described is semitransparent to light emitted from a surface light-emitting device such as a VCSEL. Embodiments of this device could be manufactured at sufficiently low temperature as to enable fabrication directly on a VCSEL wafer. The overall light absorption of polycrystalline material is lower than in amorphous or microcrystalline material, necessitating a thicker intrinsic layer in the PIN device.

The graph of quantum efficiency in Fig. 26 illustrates the relative performance of amorphous silicon 2601, microcrystalline silicon 2602 and polycrystalline silicon 2603.

No device based on a single, either crystalline or amorphous form of silicon has everything that is desirable in all layers of a semitransparent PIN photodetector. Microcrystalline and polycrystalline silicon, for instance, have lower absorption than amorphous silicon-germanium, and therefore thicker layers are required to achieve the desired responsivity. Besides higher costs and longer fabrication times, thicker films also are more likely to result in stresses in the PIN devices, possibly leading to failure during fabrication, testing, or operation. Amorphous silicon, on the other hand, is not desirable for the N- or P-layers of the PIN device precisely because it does absorb light, and additionally because it has very poor conductivity, and it is preferred that carriers generated in the I-layer be transported through low-resistance layers.

Combinations of different type of materials for the N-, I-, and P-layers of the PIN device, forming heterojunctions form devices with better overall function as semitransparent power monitors. The factors of performance, a tradeoff between responsivity, transmissivity, wavelength range, and stability, are determined on an

The semitransparent PIN device is fabricated using equipment such as that used to build amorphous silicon solar cells in large quantities. The preferred method of deposition is to use a plasma-enhanced chemical vapor deposition (PE-CVD) process:

1. Deposit a transparent conductor on a substrate that is transparent to the wavelength of interest as previously described. Because of the high hydrogen concentration used to form microcrystalline silicon, zinc oxide is preferred.

2. Without removing the substrate from vacuum during the following steps, and having the substrate at an elevated temperature, e.g., above 300°C, but as low as about 200°C for sensitive substrates, throughout the process, perform the following steps to fabricate the semiconductor detector layers. To deposit microcrystalline silicon, high hydrogen dilution, e.g., >60% by volume, and increased DC or RF power should be used for all steps.

a. Deposit a relatively thin p-doped layer of amorphous silicon using commonly-known dopant such as boron.

b. Deposit a relatively thick intrinsic layer of microcrystalline silicon. The layer thickness should be larger than its amorphous silicon counterpart because the absorption of microcrystalline silicon will be lower.

c. Deposit a relatively thin N-doped layer of amorphous silicon using a dopant such as phosphorous.

3. Deposit a transparent conductor on top of the resulting PIN stack. This conductor serves as the top contact for the device.

The completed PIN stack is depicted in Fig. 3. Microcrystalline silicon-germanium alloys, used in such a structure, would further extend the wavelengths addressable by a semitransparent PIN photodiode.

The resulting device may be employed to monitor any light source up to roughly 950nm or higher, even beyond 1,000nm. The PIN described is used in similar configurations to those described above.

Three methods to fabricate the microcrystalline PIN photodiode of the present invention are now described.

1. Fabricate a hydrogenated amorphous silicon PIN stack, using a method known to one skilled in the art, such as a chemical vapor deposition process on a transparent conductor as described above. Then recrystallize in a processing furnace at high

polyimides or the VCSEL wafer itself. Examples of completed PIN stacks are shown in Figs. 27, 28, 29 and 30.

Advanced Structures

Several more advanced structures for semitransparent optical monitoring are now described.

Advanced small-aperture PIN photodiodes, as shown in Figs. 31 and 32 minimize fabrication steps and eliminates one or both transparent conducting layers from the semitransparent PIN device. The device relies on the enhanced conductivity of microcrystalline and polycrystalline silicon over their amorphous counterpart to transport charge over a short distance in the device's N- and P-layers. These layers are contacted directly to the metal lineouts used to interface to VCSEL power control circuitry, without the transparent conductor as described above This device may include microcrystalline or polycrystalline layers either throughout the PIN device or at least for the top and bottom layers.

The structure of Fig. 31 includes, on a substrate 106, a bottom patterned metal layer 3101, the PIN stack 3102, 3103, 3104, a passivating layer 3105, and a top patterned metal layer 3106, deposited and patterned in the order given. Fig. 32 shows a similar structure, including the substrate 106, the bottom patterned metal layer 3101, the PIN stack 3102, 3103, 3104 and the passivating layer 3105. This structure further includes a top transparent conductor 3201, followed by a top metal layer 3202.

A two-level lineout and contact pad structure for tall microelectronic structures reduces connection problems in advanced devices. Specifically for PIN photodetectors, as shown in Fig. 33, the entire PIN structure can be extended 3301 under the lineout 3302 and the contact pad (not shown) in order to establish a level plane on which to deposit the metal lineout 3302 using a sputtering technique. The photodetector function remains the same, since the detector aperture 3303 is defined by the inside ring contact 3304. The advantage of this structure is that very tall photodetectors can be built in order to increase photocurrent at long wavelengths, and bottom and top line-outs may still be deposited and patterned in one step.

Making the Advanced Structures

These devices are made by the methods already described herein.

Substrates for PIN photodetectors include crystalline silicon and glass. Glass has been used extensively, for instance, in x-ray detector arrays.

Semitransparent PIN photodetectors can according to this aspect of the invention, be made on a flexible substrate in order to allow for easy integration with packaging, electronics, waveguides, and of course the VCSEL wafer. The viability of electronic devices built on such substrates for reducing package size has been extensively demonstrated in hearing aids, where polyimide printed circuits are used as integrated circuit substrates. In terms of integration with a VCSEL wafer, a flexible or compliant PIN substrate eliminates the need for an additional interfacing layer, and may simplify interconnections. In addition, direct bonding of such a substrate with the VCSEL wafer will reduce the number of layers that must be sawed over other integration schemes, and most likely improve overall device yield due to fewer alignment, stress, interconnect, and dicing issues. The PIN stacks can be produced directly on a flexible substrate which may then be integrated, or diced, then integrated, with any number of devices. Certain substrates often used in electronics manufacturing, such as Dupont's Kapton™-brand polyimide have been used extensively to provide printed circuit layers complete with layer-interconnection vias. One of these materials, for example high-temperature plastics, can be used as the substrate. Kapton™ is also transparent to the wavelengths of interest, up to roughly 900nm. Finally, certain plastics such as Kapton™ have been used to build planar waveguides. Thin-film semiconductor devices such as semitransparent PINs and other circuit elements could be integrated directly with a communications waveguide of Kapton™.

We have previously described a number of methods of fabricating thin-film PIN devices for semitransparent optical power monitoring applications. High-temperature plastics may withstand processing temperatures of up to roughly 300°C (certain plastics are advertised to 400°C), and functional arrays of devices such as transistors on polyimide foils as thin as 50 microns have been deposited by the same methods as described above. Plastics with transparent conducting and metal coatings are commercially available, clearly demonstrating that the first step of all the proposed processes is viable and even simple. The present invention is the first known example that integrates semitransparent PIN detectors with such a substrate. The excellent

As a first step in manufacturing integrated VCSEL/PIN systems (or similar systems integrating another type of surface-emitting light source), PIN devices 3401 should be formed and contacted on a flexible substrate 3402 as described above.

Upon completion of this step (and potentially burn-in and testing, as described below), a form of solder bumping 3403 could be used on either the PIN substrate 3402, the VCSEL wafer 3404, or both. These bumps 3403 will form the contacts to the VCSEL surface 3405, and potentially the common leads for the PIN and VCSEL. The PIN substrate 3402 is then aligned with and bonded to the VCSEL wafer 3404 in such as way as to line up the VCSEL apertures 3407 with the PIN apertures 3408. The PIN apertures 3408 may be sized according to the accuracy of this flip-bonding step. The pre-deposited solder bumps 3403 form contacts between the surfaces, while an adhesive such as an epoxy 3406, which should be transparent to the wavelength of interest, and should be optically matched to both the VCSEL aperture 3407 and the PIN aperture 3408 is used to bind the two surfaces together. After curing of the adhesive, vias may be drilled through the flexible PIN substrate and possibly the cured adhesive to make contact to the front VCSEL contact and the PIN contacts. The drilling process is arrested by the metal pads formed on the PIN side of the flexible substrate, or the top metal contact on the VCSEL wafer surface. Finally, these vias are filled or coated with conductor; the vias may either be connected to pre-formed metal traces on the rear side of the flexible substrate, or solder pads may be used directly as the contact for wiring, or, in a more complex system, the entire integrated device may now be flipped on to a waveguide or other transparent surface with pre-patterned contacts. It should be noted that the possibilities for the preceding steps are nearly endless because they have been extensively refined in various other applications.

According to the following method an oversized array of PIN devices is formed on a substrate in such a way that the PIN devices may be tested, either completely or through statistical sampling, and then a portion of the PIN array is bonded to a VCSEL wafer in such a way as to maximize yield and performance of the integrated devices. The oversized arrays may even be of such size that they can be used for more than one VCSEL wafer. Thin-film processes for 8" wide substrates are already common. With an 8"x8" substrate, it is theoretically possible to build 16 integrated VCSEL/PIN wafers based on 2" wafers, as used by some VCSEL manufacturers today. Alternatively, fewer

plug-out connector, transmitters or transmitter arrays that are flipped directly on to planar optical waveguides, and of course replacements for current VCSEL/backreflection photodiode systems.

Integrated power monitoring devices with VCSELs or similar devices have not yet been commercialized because of at least two factors: (1) the difficulty of producing a thin-film photodetector with adequate photoresponse and low dark current that also transmits a majority of the light being emitted by the VCSEL; and (2) the relatively high temperatures at which conventional thin-film processing is performed combined with the VCSEL wafer's sensitivity to high temperatures. Processed VCSELs are sensitive to high temperatures, primarily because of the large number of layers that make up their internal reflectors. At each of the interfaces within the VCSEL there is already an inherent strain due to crystal lattice mismatches. These strains are aggravated by large temperature swings, actually demonstrable by the change in laser output as temperature rises. VCSEL manufacturers have indicated 200-300°C as a maximum for follow-on processing on a VCSEL wafer. The majority of the fabrication methods described above can be implemented using low-temperature techniques, thereby enabling direct integration with VCSEL wafers.

The semitransparent photodetector should be built, as shown in Fig. 37, in such a way as to reflect a minimum amount of light back into the VCSEL aperture to avoid negative interactions with the laser itself. This means that the detector 3701 should be positioned in such a way that it minimizes optical interaction with the VCSEL 3702; and the thickness and index of refraction of layers 3703 between the VCSEL aperture 3704 and the top of the photodiode should be selected in such a way as to minimize reflectance. The semitransparent photodetector 3701 could also be purposely built as a resonant cavity in tune with the VCSEL. This, however, involves much more tuning and will result in a more expensive manufacturing process. Therefore, the exemplary device has a relatively thick layer 3705 between the VCSEL 3702 and the PIN detector 3701. This layer 3705 reduces the optical effects mentioned above, forms a substrate for the PIN device 3701, acts as an insulator between VCSEL and PIN contacts 3706, 3707, and reduces the capacitance induced by the layering of devices, which may be an important determinant of VCSEL switching speed.

output power. The total thickness of the resulting package can be thin enough that the majority of the VCSEL beam, after passing through the optical power monitoring layer, enters the core of the waveguide at an appropriate angle. Where the VCSEL divergence angle is high or the waveguide core diameter is particularly small, as would be the case with a singlemode fiber, additional flat optics may be used to guide light into the waveguide; our focus, however, is on multimode systems operating at wavelengths under roughly 1000nm where the core diameter is relatively large and no additional optics must be integrated. If a lens must be integrated, it may be beneficial to do this using a graded-index lens which can be constructed in a flat package. Commercially-available VCSEL chips have beam divergences of under 20°, and as low as 10°. In its most basic implementation this aspect of the present invention consists of three layers closely packed together: (1) a VCSEL or VCSEL array; (2) an semitransparent optical power monitor such as a PIN photodetector; and (3) a waveguide such as an optical fiber or a planar polymer waveguide. The components may be in several configurations. Examples of a few include: (1) semitransparent optical power monitor 3801 fabricated directly on, or flip-bonded to, the VCSEL 3802 or VCSEL array and covered with a transparent protective coating 3803 which is polished and interfaced to a waveguide 3804, as shown in Fig. 38, which is potentially connectorized in such a manner is to be easily pluggable, (2) semitransparent optical power monitor fabricated directly on the waveguide aperture, with the VCSEL or VCSEL array flip-bonded onto the waveguide for a permanent connection, as shown in Fig. 39. Several other configurations are potentially possible; all will have the form of a stack of closely-packed components including a VCSEL, a semitransparent optical power monitor, and a waveguide arranged in such a manner that the majority of the light emitted by the VCSEL and passed through the optical power monitor reaches the effective area of the waveguide.

Many options for manufacturing and packaging this embodiment of the present invention exist. An integrated package generally requires a certain amount of electrical, optical, and mechanical bonding, which are best achieved, as detailed above using optical epoxies and well-known flip-bonding techniques. Fig. 40 shows one potential implementation where the integrated VCSEL-PIN photodetector package has been manufactured using the processes described above. The resulting diced unit, either in single-VCSEL or VCSEL array form is mounted on a substrate for wirebonding. The

The waveguide is formed with a cleaved edge so as to reflect light arriving perpendicular to its plane (from a flipped VCSEL array) into rectangular waveguides running in its plane. These waveguides are then fanned out and interfaced to using a standard connector, such as AMP's LightRay™ MPX system, to an array of fibers. If power control is required, as it is when the link is to be high speed and eye-safe, the only alternative prior to the present invention was to use an array of individual VCSELs, each packaged in a TO can with a semireflective window and a backreflection optical power monitor. Besides the massive cost increase over a solution based on embodiments of the solution proposed above as enabled by the present invention, the space requirement is enormous by comparison, drastically reducing applicability in real-world systems. A practical implementation of this system using the present invention is depicted in Fig. 36. Finally, the present invention can be used with many emerging and future technologies. An integrated power monitoring solution for one of these -- coarse wave division multiplexing -- is shown in Fig. 37. In this system, VCSEL arrays in which VCSELs are tuned to different wavelengths or are tunable during operation, are used to send signals of multiple wavelengths over a single waveguide. Light emitted from the flipped VCSEL array is directed through the semitransparent PIN detector array into the waveguide plane, and subsequently to merge the individual waveguides, and thereby wavelengths, into a single channel using an integrated wavelength multiplexer structure. This format, and many other systems that are proposed or under development, stand to gain significantly from embodiments of the present invention through its ability to reduce costs, package size, and complexity while enhancing switching speeds and eye safety.

The present invention has now been described in connection with a number of specific embodiments thereof. However, numerous modifications, which are contemplated as falling within the scope of the present invention, should now be apparent to those skilled in the art. Therefore, it is intended that the scope of the present invention be limited only by the scope of the claims appended hereto.

What is claimed is:

8. The method of claim 7, further comprising:
doping the P layer with boron.

9. The method of claim 7, further comprising:
doping the N layer with phosphorous.

10. The method of claim 7, further comprising:
bonding the substrate to a vertical cavity surface emitting laser (VCSEL) device.

11. The method of claim 7, wherein the substrate is a layer of a vertical cavity surface emitting laser (VCSEL) device.

12. The method of claim 7, further comprising:
integrating the substrate in a package for a laser device, in a light path of the laser.

13. The method of claim 7, further comprising:
varying a concentration of GeH_4 gas in the chemical vapor deposition gas to vary introduction of germanium into the alloy from a relatively low concentration for deposition at a boundary with the P layer, to a high concentration for deposition within the I layer, and to a relatively low concentration for deposition at a boundary with the N layer.

14. The method of claim 13, wherein the low concentration of GeH_4 gas is about 0% of the chemical vapor deposition gas and the high concentration of GeH_4 gas is selected to optimize photon absorption at a wavelength of interest.

15. The method of claim 13, wherein the low concentration of GeH_4 gas is about 0% of the chemical vapor deposition gas and the high concentration of GeH_4 gas is about 100% of the chemical vapor deposition gas.

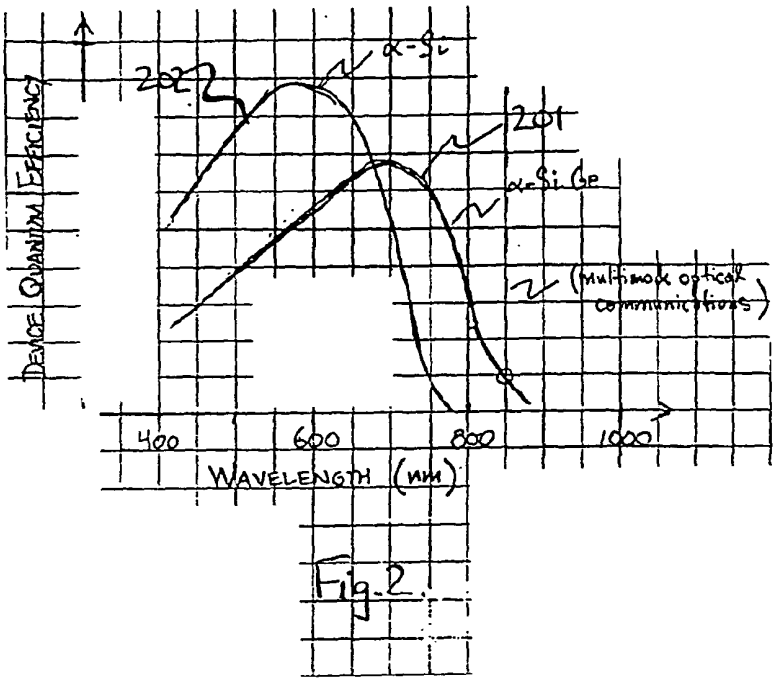
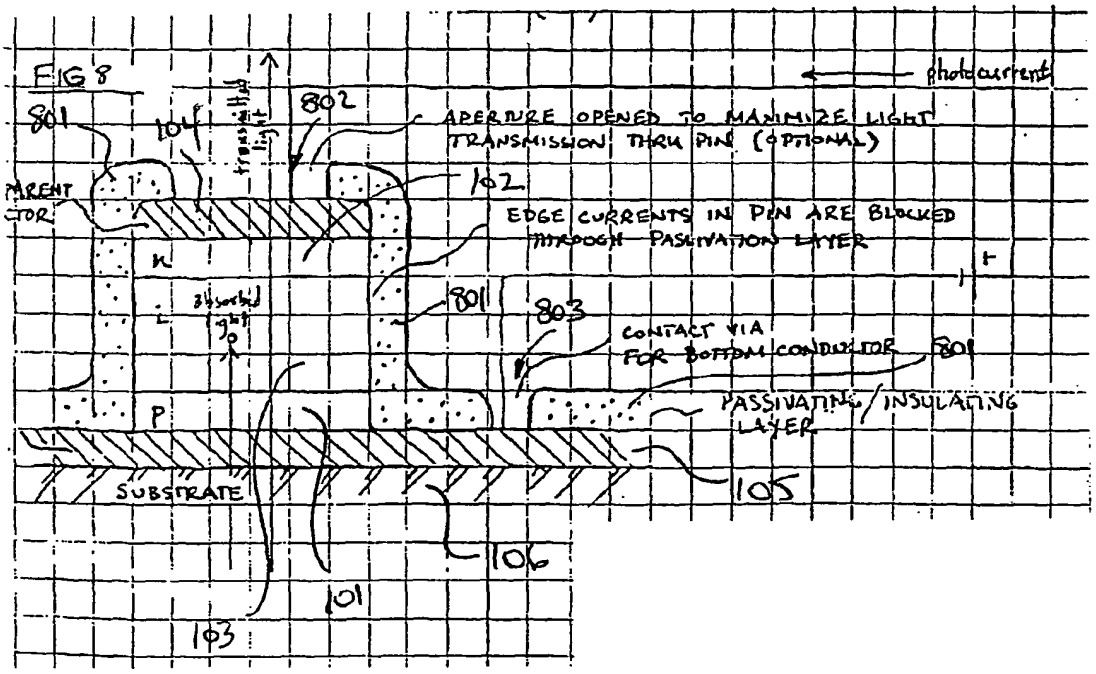
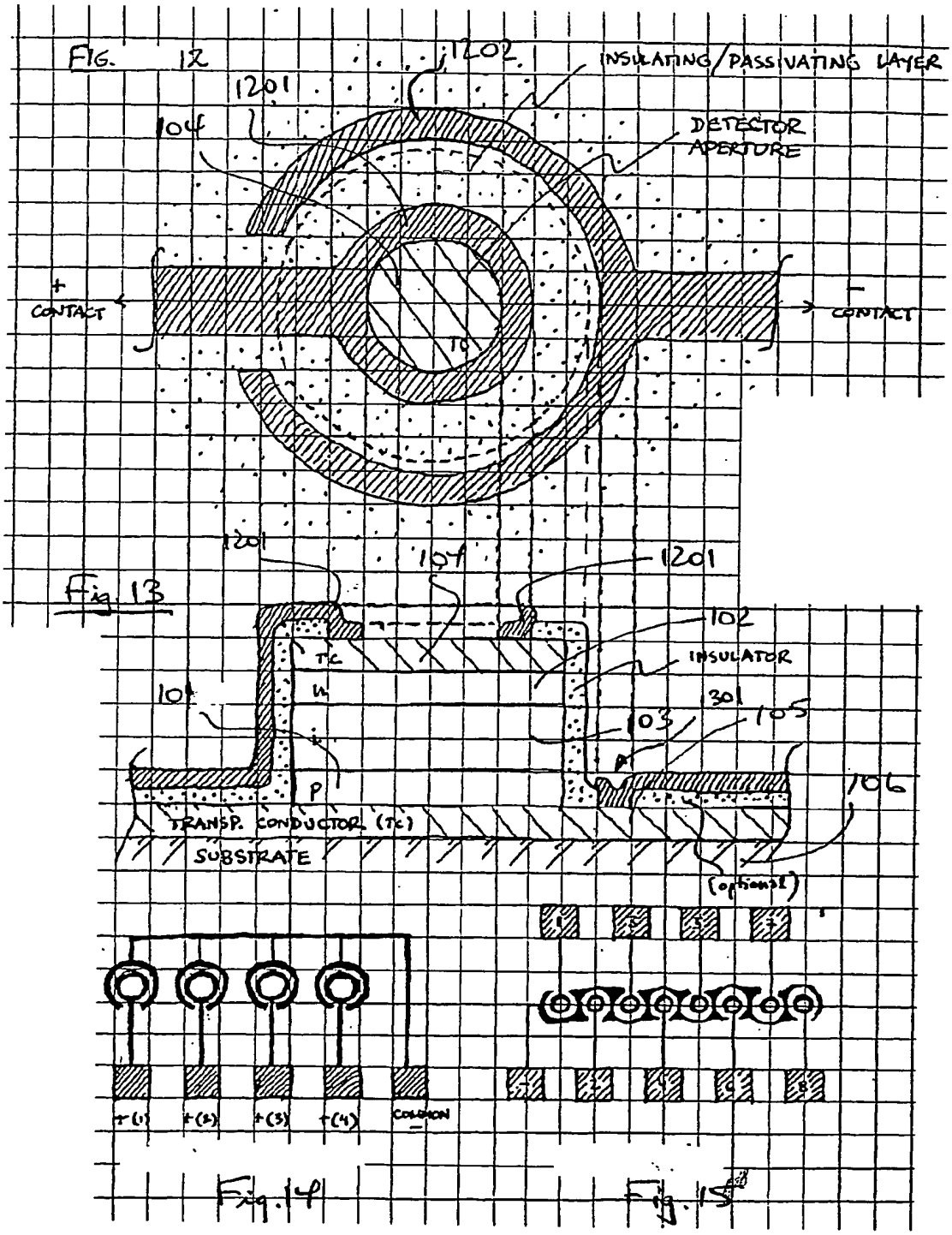
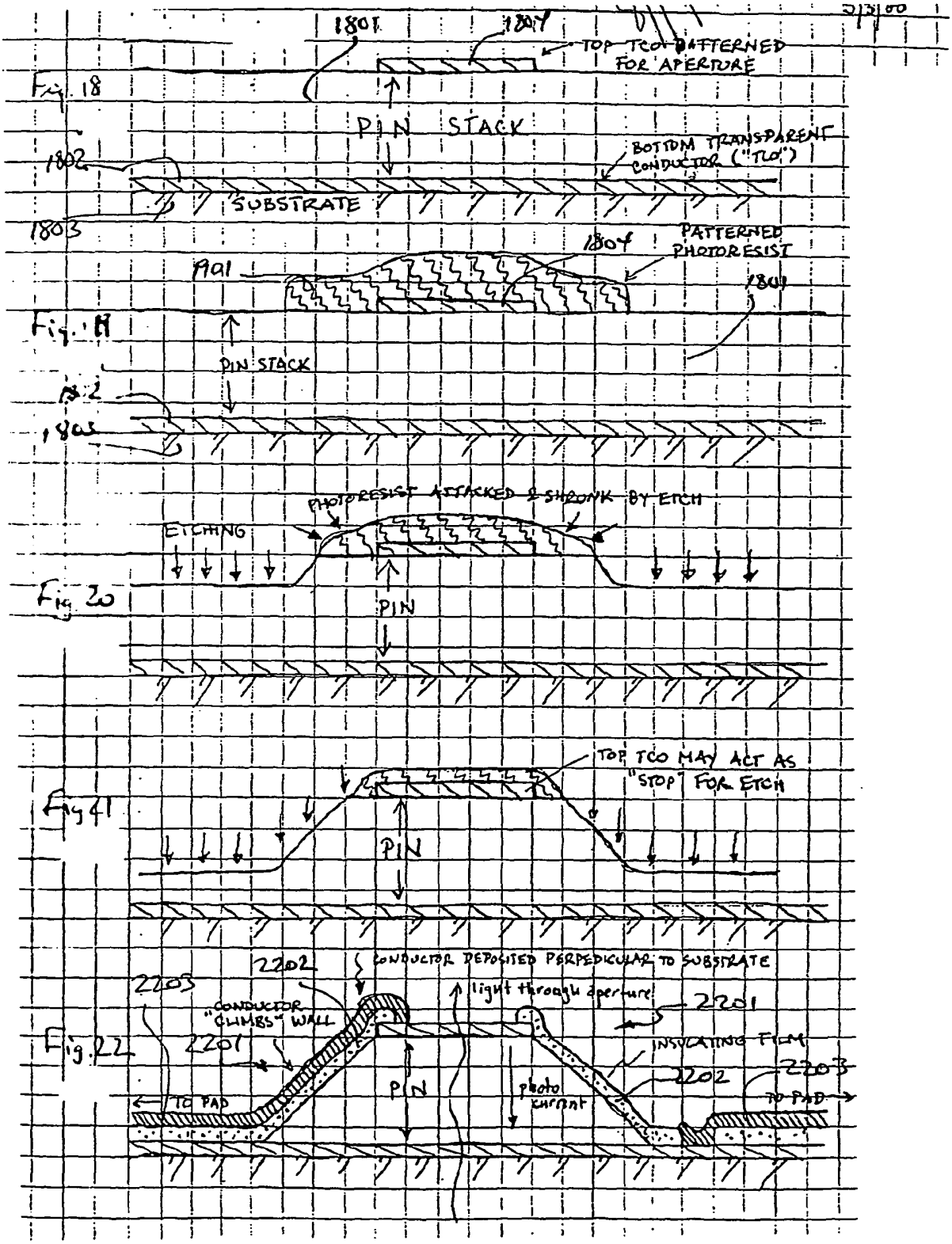

DEVICE QUANTUM EFFICIENCY
202
α-Si
201
α-Si Ge
(Multimode optical communications)
400
600
800
1000
WAVELENGTH (nm)

Fig. 2.







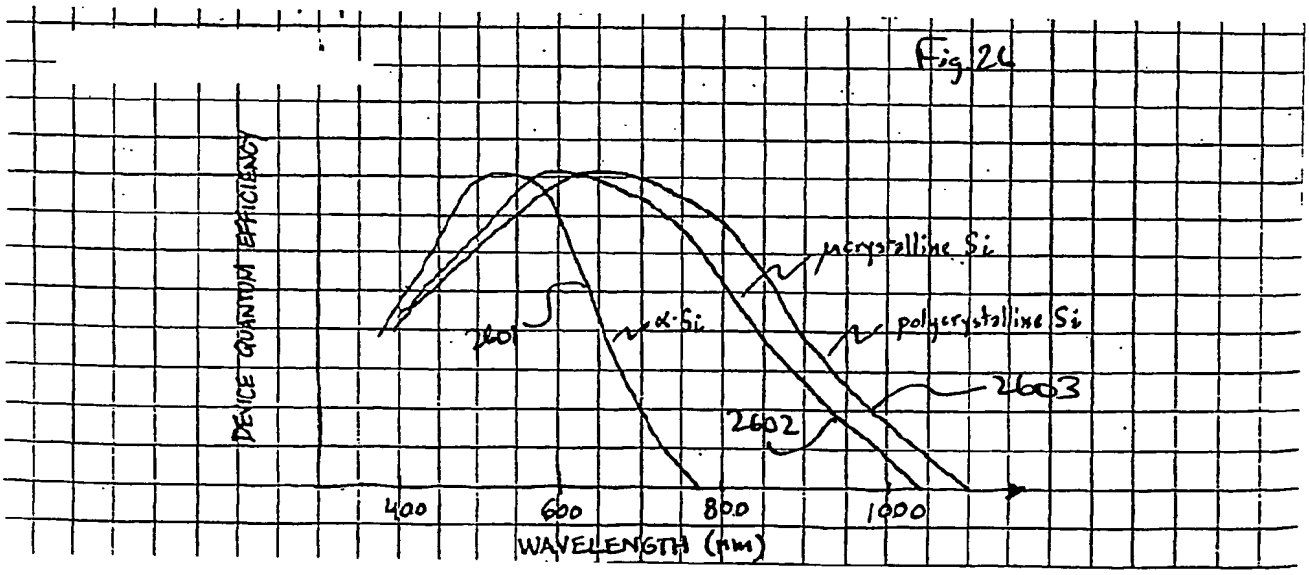
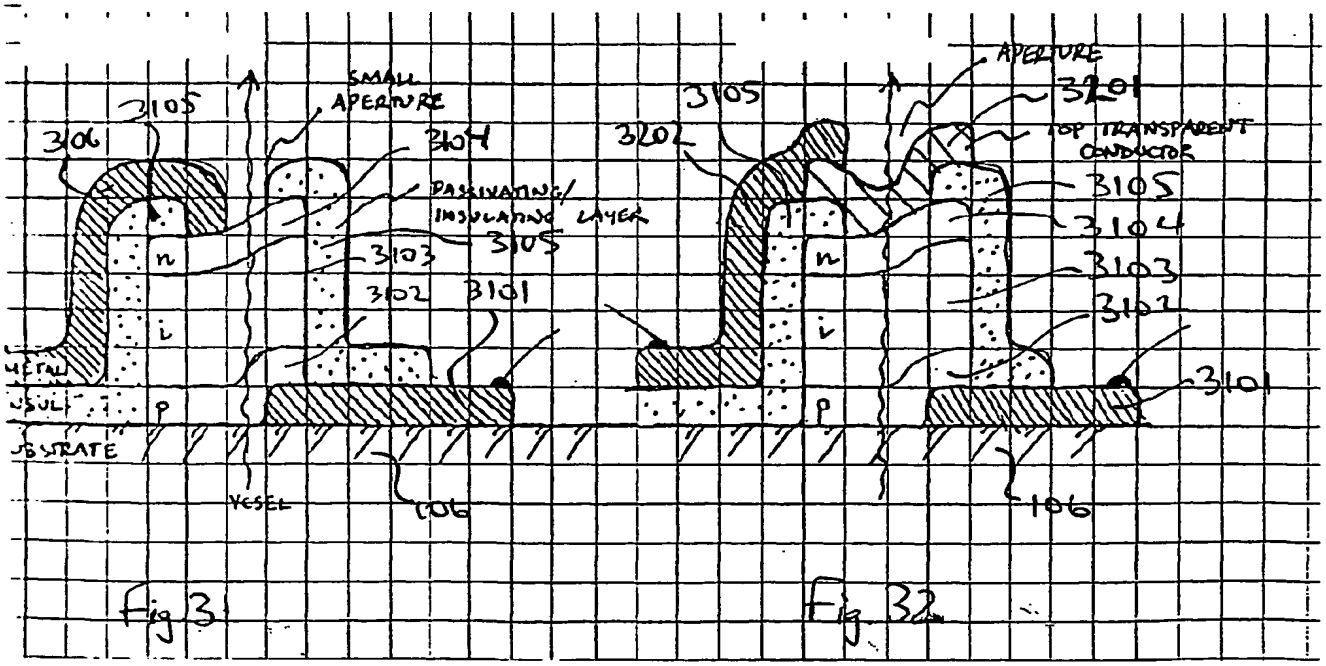


Fig 26
DEVICE QUANTUM EFFICIENCY
WAVELENGTH (nm)
400
600
800
1000
2601
α-Si
microcrystalline Si
polycrystalline Si
2603
2602


3105
3106
SMALL APERTURE
3104
PASSIVATING/ INSULATING LAYER
3105
3103
3102
3101
n
i
p
SUBSTRATE
VESSEL
106
Fig 31
APERTURE
3201
3105
3202
TOP TRANSPARENT CONDUCTOR
3105
3104
3103
3102
3101
106
Fig 32

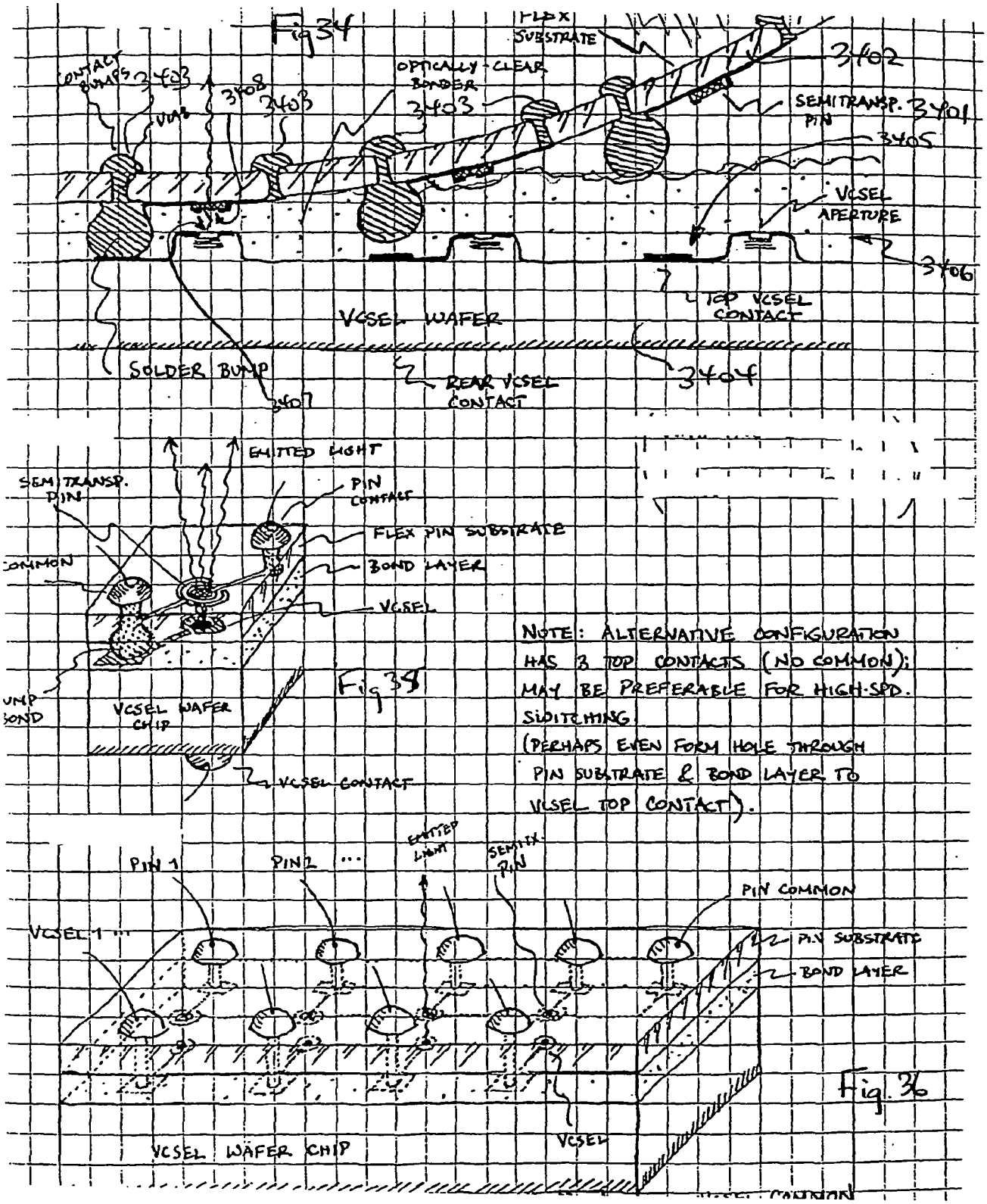


Fig 34
FLEX SUBSTRATE
3402
CONTACT BUMPS
3403
VIAS
3408
3403
OPTICALLY CLEAR BONDER
3403
SEMITRANSP. PIN
3404
3405
VCSEL APERTURE
3406
TOP VCSEL CONTACT
VCSEL WAFER
SOLDER BUMP
3407
REAR VCSEL CONTACT
3404
EMITTED LIGHT
SEMITRANSP. PIN
PIN CONTACT
FLEX PIN SUBSTRATE
BOND LAYER
VCSEL
COMMON
BUMP BOND
VCSEL WAFER CHIP
VCSEL CONTACT
Fig 35
NOTE: ALTERNATIVE CONFIGURATION HAS 3 TOP CONTACTS (NO COMMON); MAY BE PREFERABLE FOR HIGH-SPD. SWITCHING. (PERHAPS EVEN FORM HOLE THROUGH PIN SUBSTRATE & BOND LAYER TO VCSEL TOP CONTACT).
PIN 1
PIN 2 ...
EMITTED LIGHT
SEMITR. PIN
PIN COMMON
VCSEL 1 ...
PIN SUBSTRATE
BOND LAYER
Fig. 36
VCSEL WAFER CHIP
VCSEL

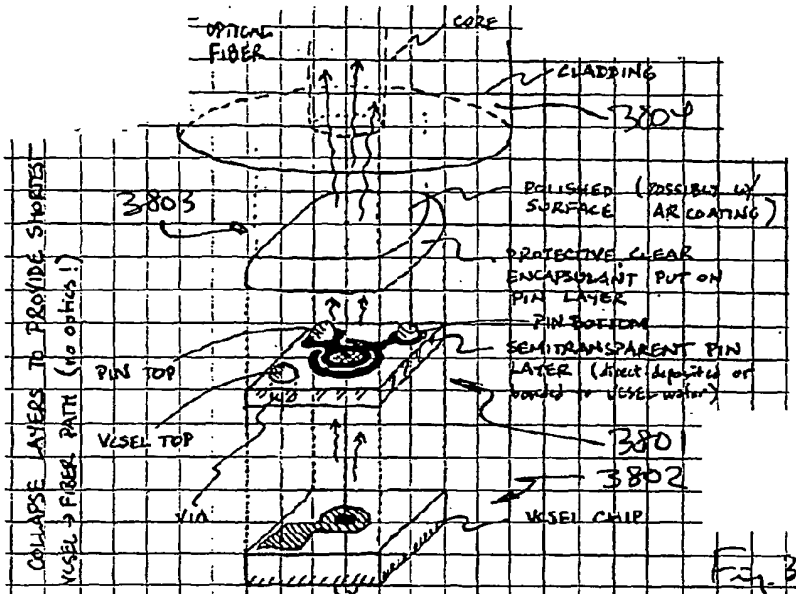


Fig. 38

.. SUCH A PACKAGE WOULD ALLOW LOW-COST DIRECT COUPLING IN A FIBER CONNECTOR (VCSEL APERTURE < 25μm AND MULTIMODE FIBER CORE ≠ 50-62.5μm; VCSEL BEAM DIVERGENCE ≤ 20°, AND PIN LAYER IS THIN).

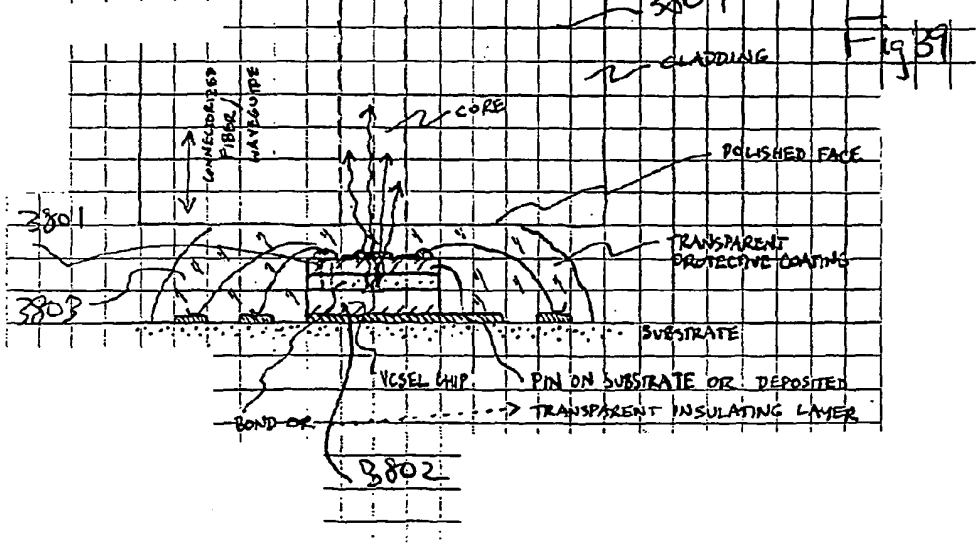


Fig. 39